a field isolation region separating active regions, wherein said field isolation region includes an isolation trench, said isolation trench further including a first area filled with a first dielectric material forming at least sidewalls of said isolation trench, and a second area filled with a second dielectric material situated within said sidewalls; and

an ion implanted region of said semiconductor substrate below said second area, substantially all ions from said ion implanted region being displaced away from said separated active regions.

69. The integrated circuit of claim 68 wherein said first area also includes said first dielectric material provided on a bottom of said isolation trench and said second dielectric material provided over said first dielectric material provided at said bottom.

70. The integrated circuit of claim 68 wherein said ions from said ion implanted region are displaced away from said separated active regions by a distance at least equal to a sidewall thickness of said first area.

71. The integrated circuit of claim 68 wherein said first dielectric material and said second dielectric material are the same.

72. The integrated circuit of claim 68 wherein said first dielectric material and said second dielectric material are different.

73. A memory device comprising:

a semiconductor substrate including a plurality of active regions; and

a field isolation region separating adjacent active regions, said field isolation region including an isolation trench, said isolation trench further including a first area filled with a first dielectric material forming at least sidewalls of said isolation trench, and a second area filled with a second dielectric material situated within said sidewalls, and an ion implanted region of said semiconductor substrate below said second area, substantially all ions from said ion implanted region being displaced away from said active regions by a distance at least equal to a sidewall thickness of said first area filled with said first dielectric material.

74. The memory device of claim 73 wherein said first area also includes said first dielectric material provided on a bottom of said isolation trench and said second dielectric material provided over said first dielectric material provided at said bottom.

75. The memory device of claim 73 wherein said first dielectric material and said second dielectric material are the same.

76. The memory device of claim 73 wherein said first dielectric material and said second dielectric material are different. --

Please amend the following claims:

45. The integrated circuit of claim [43] 68 wherein substantially all the ions are displaced from [the] said separated active regions by at least one hundred angstroms.

46. The integrated circuit of claim [43] 68 wherein [the] said separated active regions include elements of a memory device.

Claim 49, line 1, change "43" to --68--.

Claim 50, line 1, change "43" to --68--.

51. The integrated circuit of claim [43] 68 wherein the ions are implanted into the substrate below [the dielectric-filled area] said first area filled with said first dielectric material to a depth in a range of about 10 to 100 percent the depth of [the dielectric-filled area] said first area filled with said first dielectric material.

52. The integrated circuit of claim [43] 68 wherein the ions are implanted into the substrate below [the dielectric-filled area] said first area filled with said first dielectric material to a depth in a range of about 20 to 80 percent the depth of [the dielectric-filled area] said first area filled with said first dielectric material.

Claim 54, line 1, change "53" to --73--.

55. The memory device of claim [53] 73 wherein the sidewall thickness of [the first dielectric regions] said first area filled with said first dielectric material is less than about forty percent the width of the isolation region.

Claim 57, line 1, change "53" to --73--.

59. The memory device of claim [53] 73 wherein the ions are implanted into the substrate below [the dielectric-filled area] said first area filled with said first dielectric material to a depth in a range of about 10 to 100 percent the depth of [the dielectric-filled area] said first area filled with said first dielectric material.